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Search Results -

Terms	Documents
L3 and (alignment near2 structure)	4

Database:
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

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Recall Text Clear Interrupt

Search History

DATE: Monday, January 24, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L4	L3 and (alignment near2 structure)	4	L4
L3	L2 and optical and reflectiv?	121	L3
L2	L1 and laser	1194	L2
L1	pld or (programmable adj logic adj device)	7689	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6624524 B1

L4: Entry 1 of 4 File: USPT Sep 23, 2003

US-PAT-NO: 6624524
DOCUMENT-IDENTIFIER: US 6624524 B1

TITLE: Laser alignment target

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 6339459 B1

L4: Entry 2 of 4 File: USPT Jan 15, 2002

US-PAT-NO: 6339459
DOCUMENT-IDENTIFIER: US 6339459 B1
** See image for Certificate of Correction **

TITLE: Liquid crystal display device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 3. Document ID: US 6002182 A

L4: Entry 3 of 4 File: USPT Dec 14, 1999

US-PAT-NO: 6002182
DOCUMENT-IDENTIFIER: US 6002182 A

TITLE: Laser alignment target

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 4. Document ID: US 5998295 A

L4: Entry 4 of 4 File: USPT Dec 7, 1999

US-PAT-NO: 5998295
DOCUMENT-IDENTIFIER: US 5998295 A

TITLE: Method of forming a rough region on a substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw D

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Terms	Documents
L3 and (alignment near2 structure)	4

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

L4: Entry 1 of 4 File: USPT Sep 23, 2003

DOCUMENT-IDENTIFIER: US 6624524 B1
TITLE: Laser alignment target

Abstract Text (1):
A technique to form a structure with a rough topography (415) in a planarized semiconductor process. The rough topography (415) is formed by creating cored contacts (433). Subsequent process layers may be further stacked on top of the cored contacts in order to augment nonplanar characteristics of the cored contacts. This rough topography structure may be used to align integrated circuits and wafers. An integrated circuit may be laser aligned using this alignment structure.

Brief Summary Text (5):
Moreover, alignment is also important when programming or configuring an integrated circuit. For example, a die may have fuses that are to be laser programmed. The fuses may be made of polysilicon, or another conductor. This fuse may couple together two (or more) devices or conductors. A laser with sufficient energy is directed at the fuse. The laser "blows" the fuse, decoupling the two devices or conductors. In order for the laser to properly reference the coordinates of a fuse, the integrated circuit must be aligned properly. When the integrated circuit is not aligned properly, the laser may damage or destroy a portion of the circuitry instead of blowing the desired fuse. Therefore, the alignment of an integrated circuit or wafer is especially critical.

Brief Summary Text (7):
One technique of alignment is by use of an alignment target. An alignment target should have good reflective or optical contrast so it can be easily identifiable. For example, a laser may be used to determine a change in reflectivity or optical contrast in a semiconductor structure used as the alignment target. This contrast may be achieved by forming a region with rough topography and a region with a smooth topography, where these regions are in close proximity to one another. Light is reflected from the smooth or planar region while light is scattered from the rough region. A laser alignment system would find this alignment target and align the wafer or integrated circuit based on the target.

Brief Summary Text (9):
Despite the substantial success of such planarized process technologies, these processes also meet with certain limitations, especially when used to create a region having good reflectivity, which may be used as an alignment target. With flat or smooth topographies, the resulting structures and regions will have a similar optical reflectiveness. This leads to poor reflective or optical contrast, making it difficult (and possibly impossible) to align a wafer or integrated circuit die, especially by using laser. Furthermore, in some processes, metals use antireflective coatings, further reducing the reflectivity contrast over flat topography.

Brief Summary Text (10):
As can be seen, a structure and technique for fabricating a good reflective contrast is needed, especially where this structure is useful as an alignment target for aligning a wafer or integrated circuit.

Brief Summary Text (12):
The present invention is a structure and technique for fabricating a structure having good reflective contrast for use as an alignment structure. In particular, a technique of the present invention is for fabricating a structure having a rough topography using a planarized semiconductor process. The rough topography structure of present invention has a different reflectivity compared to a smooth or planar topography structure. Specifically, the rough topography will scatter incident radiation and light, while the smooth topography will reflect radiation and light. A structure including both rough and smooth topographies may be used as an alignment target for aligning an integrated circuit or wafer. The system will be able to identify the reflective and optical contrast between the smooth and rough topography. After alignment, an integrated circuit, such as a memory, microprocessor, or programmable logic device, may be programmed, such as by a laser to blow laser-programmable fuses.

Brief Summary Text (15):
Moreover, an alignment structure for semiconductor fabrication of the present invention includes a smooth and a rough region formed on a substrate. The rough region includes a first conductive layer and a second conductive layer formed above the first conductive layer. A first insulating layer is formed between the first and second conductive layers. The first insulating layer has a first opening for electrically coupling the first and second conductive layers. A plug layer, having a cored region, fills the first opening. The topographical roughness formed by the cored region scatters incident radiation.

Drawing Description Text (4):
FIG. 2A shows a top view of an alignment structure of the present invention;

Drawing Description Text (5):
FIG. 2B shows a top view of another embodiment of an alignment structure of the present invention;

Drawing Description Text (7):
FIG. 4 shows a cross-section of an alignment structure of the present invention;

Detailed Description Text (2):
FIG. 1 is a diagram of an integrated circuit 110 and alignment targets 120. Integrated circuit 110 may be one of many on a wafer. Alignment targets 120 are used to align the integrated circuit. For example, alignment targets 120 may be used in the laser alignment of integrated circuit 110. Alignment targets 120 may also be used to align other objects and structures, such as entire wafers.

Detailed Description Text (8):
A particular application, among many others, where alignment of integrated circuits is especially important is the laser programming of fuses within the dies. As shown in FIG. 1, there may be one of more fuses 130 within the integrated circuit. Each may control a particular feature. For example, fuse-programmable options may be used to repair against low-level defects in integrated circuits. If a defect is found in a particular circuit, then after the integrated circuit has been aligned using the alignment targets, a laser is referenced to a selected fuse location with the integrated circuit. The laser "blows" the fuse, which may be made of polysilicon or metal, in order to enable or disable the appropriate circuitry.

Detailed Description Text (9):
Alignment is especially critical since the laser must properly reference the precise location on the integrated circuit to program the fuse. For example, fuses may occupy less than 100 square micron area. Any misalignment error, and the laser may damage a portion of the integrated circuit.

Detailed Description Text (10):

Laser programming may also be employed in implementing redundancy of integrated circuit chips. With redundancy, some defective elements of a die can be replaced with nondefective extra resources provided for the repair. The accuracy of the replacement depends on the accuracy of laser programming.

Detailed Description Text (11):
Laser programming may be useful for configuring various types of integrated circuits including, but not limited to, memories, microprocessor, ASICs, gate arrays, field programmable gate arrays (FPGAs), and programmable logic devices (PLDs). For example, for PLDs, laser programming may be used to configure the logical elements and interconnections within between the logical elements. PLDs are typically programmed by electrically programming fuses, antifuses, EPROM, Flash, EEPROM, or SRAM cells.

Detailed Description Text (12):
Programmable logic integrated circuits and their operation are well known to those of skill in the art. See, for example, U.S. Pat. No. 4,617,479, incorporated herein by reference for all purposes. Such devices are currently represented by, for example, Alterals MAX.RTM. series of PLDs and FLEX.RTM. series of PLDs. The former are described in, for example, U.S. Pat. Nos. 5,241,224 and 4,871,930, and the Altera Data Book, March 1995, all incorporated herein by reference. The latter are described in, for example, U.S. Pat. Nos. 5,258,668, 5,260,610, 5,260,611 and 5,436,575, and also the Altera Data Book, March 1995, all incorporated herein by reference for all purposes.

Detailed Description Text (13):
Laser programming may be used in place of, or to supplement, the electrical configuration of PLDs. For example, laser programming may be used to program the programmable interconnect array (PIA), global interconnect, local interconnect, and other interconnection within a PLD. Laser programming.may also be used to configure the functionality of logic array blocks (LABs) and logic elements (LEs). As a further example, a look-up table in a PLD may be configured by the way of laser programming.

Detailed Description Text (14):
The integrated circuit may be programmed in part by laser programming, then further electrically configured or programmed by a user. The user may program the device using a programmer device or using in-system programming (ISP). ISP involves electrically programming an integrated circuit while it resides on a system board. For example, a laser may program a portion of the global interconnect; and if desirable or necessary, the remaining portion of the global interconnect is configured in the field (i.e., by a customer or user).

Detailed Description Text (15):
Laser programming may be used to implement some features which are typically implemented using mask-programmable options. Mask-programmable options are features of the integrated circuit which are enabled or disabled by using an appropriate mask during a masking step. These options are usually implemented during a metal masking step, such as first or second metal layers. Although mask-programmable options are an effective technique, laser programming offers many advantages. For example, among other advantages, laser programming may lower overall production cost since integrated circuit dies do not need to be laser programmed until just before the parts are needed. Generic (unconfigured) parts may be stored in inventory and laser configured as needed. This eliminates the need of keeping an inventory in various customized and specialized products.

Detailed Description Text (17):
Alignment target 210 includes a rough topography 220 and a smooth topography 230. Rough topography 220 and smooth topography 230 have a dissimilar optical reflectiveness. Generally, smooth topography 230 reflects incident radiation or

L4: Entry 4 of 4 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5998295 A
TITLE: Method of forming a rough region on a substrate

Abstract Text (1):
A technique to form a structure with a rough topography (415) in a planarized semiconductor process. The rough topography (415) is formed by creating cored contacts (433). Subsequent process layers may be further stacked on top of the cored contacts in order to augment the nonplanar characteristics of the cored contacts. This rough topography structure may be used to align integrated circuits and wafers. An integrated circuit may be laser aligned using this alignment structure.

Brief Summary Text (5):
Moreover, alignment is also important when programming or configuring an integrated circuit. For example, a die may have fuses that are to be laser programmed. The fuses may be made of polysilicon, or another conductor. This fuse may couple together two (or more) devices or conductors. A laser with sufficient energy is directed at the fuse. The laser "blows" the fuse, decoupling the two devices or conductors. In order for the laser to properly reference the coordinates of a fuse, the integrated circuit must be aligned properly. When the integrated circuit is not aligned properly, the laser may damage or destroy a portion of the circuitry instead of blowing the desired fuse. Therefore, the alignment of an integrated circuit or wafer is especially critical.

Brief Summary Text (7):
One technique of alignment is by use of an alignment target. An alignment target should have good reflective or optical contrast so it can be easily identifiable. For example, a laser may be used to determine a change in reflectivity or optical contrast in a semiconductor structure used as the alignment target. This contrast may be achieved by forming a region with rough topography and a region into a smooth topography, where these regions are in close proximity to one another. Light is reflected from the smooth or planar region while light is scattered from the rough region. A laser alignment system would find this alignment target and align the wafer or integrated circuit based on the target.

Brief Summary Text (9):
Despite the substantial success of such planarized process technologies, these processes also meet with certain limitations, especially when used to create a region having good reflectivity, which may be used as an alignment target. With flat or smooth topographies, the resulting structures and regions will have a similar optical reflectiveness. This leads to poor reflective or optical contrast, making it difficult (and possibly impossible) to align a wafer or integrated circuit die, especially by using laser. Furthermore, in some processes, metals use antireflective coatings, further reducing the reflectivity contrast over flat topography.

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As can be seen, a structure and technique for fabricating a good reflective

contrast is needed, especially where this structure is useful as an alignment target for aligning a wafer or integrated circuit.

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The present invention is a structure and technique for fabricating a structure having good reflective contrast for use as an alignment structure. In particular, a technique of the present invention is for fabricating a structure having a rough topography using a planarized semiconductor process. The rough topography structure of present invention has a different reflectivity compared to a smooth or planar topography structure. Specifically, the rough topography will scatter incident radiation and light, while the smooth topography will reflect radiation and light. A structure including both rough and smooth topographies may be used as an alignment target for aligning an integrated circuit or wafer.

Brief Summary Text (13):
The system will be able to identify the reflective and optical contrast between the smooth and rough topography. After alignment, an integrated circuit, such as a memory, microprocessor, or programmable logic device, may be programmed, such as by a laser to blow laser-programmable fuses.

Brief Summary Text (16):
Moreover, an alignment structure for semiconductor fabrication of the present invention includes a smooth and a rough region formed on a substrate. The rough region includes a first conductive layer and a second conductive layer formed above the first conductive layer. A first insulating layer is formed between the first and second conductive layers. The first insulating layer has a first opening for electrically coupling the first and second conductive layers. A plug layer, having a cored region, fills the first opening. The topographical roughness formed by the cored region scatters incident radiation.

Drawing Description Text (3):
FIG. 2A shows a top view of an alignment structure of the present invention;

Drawing Description Text (4):
FIG. 2B shows a top view of another embodiment of an alignment structure of the present invention;

Drawing Description Text (6):
FIG. 4 shows a cross-section of an alignment structure of the present invention;

Detailed Description Text (2):
FIG. 1 is a diagram of an integrated circuit 110 and alignment targets 120. Integrated circuit 110 may be one of many on a wafer. Alignment targets 120 are used to align the integrated circuit. For example, alignment targets 120 may be used in the laser alignment of integrated circuit 110. Alignment targets 120 may also be used to align other objects and structures, such as entire wafers.

Detailed Description Text (8):
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precise location on the integrated circuit to program the fuse. For example, fuses may occupy less than 100 square micron area. Any misalignment error, and the laser may damage a portion of the integrated circuit.

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Laser programming may be used to implement some features which are typically implemented using mask-programmable options. Mask-programmable options are features of the integrated circuit which are enabled or disabled by using an appropriate mask during a masking step. These options are usually implemented during a metal masking step, such as first or second metal layers. Although mask-programmable options are an effective technique, laser programming offers many advantages. For example, among other advantages, laser programming may lower overall production cost since integrated circuit dies do not need to be laser programmed until just before the parts are needed. Generic (unconfigured) parts may be stored in inventory and laser configured as needed. This eliminates the need of keeping an inventory in various customized and specialized products.